	L #	Hits	Search Text	DBs	Time Stamp
1	L1	20334	"Advanced micro devices"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/06/16 15:15
2	L2	17661	"Advanced micro devices".As.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/06/16 15:15
3	L3	240	2 and fuse	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/06/16 15:16

	L #	Hits	Search Text	DBs	Time Stamp
4	L4	2	3 and (NiSi or "NiSi.sub.2" or (mononickel near silicide) or (nikel near disilicide))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/06/16 15:22
5	L5	47	("4745079" | "4755478" | "5006913" | "5061647" | "5164805" | "5210435" | "5283455" | "5371391" | "5567966" | "5593909" | "5600168" | "5621236" | "5625217" | "5693549" | "5717237" | "5756365" | "5770490" | "5834797" | "5894157" | "5960270" | "5962895" | "5977591" | "6043545" | "6049114" | "6087208" | "6097070" | "6107667" | "6204137" | "6210999" | "6218276" | "6225669" | "6281559" | "6297106" | "6300177" | "6300657" | "6344675" | "6348387" | "6373668" | "6380589" | "6424009" | "6441433" | "6486080" | "6509612" | "6632714" | "6660588" | "6734510" | "6812514").PN.	US-PGPUB; USPAT; USOCR	2005/06/16 15:19
6	L6	0	("6888198").URPN.	USPAT	2005/06/16 15:20

	L #	Hits	Search Text	DBs	Time Stamp
7	L8	0	7 and fuse	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/06/16 15:22
8	L9	0	5 and fuse	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/06/16 15:22
9	L7	3	5 and (NiSi or "NiSi.sub.2" or (mononickel near silicide) or (nikel near disilicide))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/06/16 15:24

	L #	Hits	Search Text	DBs	Time Stamp
10	L10	174	fuse and (NiSi or "NiSi.sub.2" or (mononickel near silicide) or (nikel near disilicide))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/06/16 15:37
11	L11	33	10 and (programmed or programming or program)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/06/16 15:25
12	L12	33	11 and (voltage or current)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/06/16 15:25

	L #	Hits	Search Text	DBs	Time Stamp
13	L13	31	12 and ((@ad<"20031205") or (@rlad<"20031205"))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/06/16 15:26
14	L14	31	13 and resistance	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/06/16 15:36
15	L15	2252	xiang.in.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/06/16 15:37

	L #	Hits	Search Text	DBs	Time Stamp
16	L16	1	15 and fuse and (NiSi or "NiSi.sub.2" or (mononickel near silicide) or (nikel near disilicide))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/06/16 15:38
17	L17	326	(438/132).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/06/16 15:37
18	L18	222	(438/467).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/06/16 15:38

	L #	Hits	Search Text	DBs	Time Stamp
19	L19	489	17 or 18	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/06/16 15:38
20	L20	4	19 and fuse and (NiSi or "NiSi.sub.2" or (mononickel near silicide) or (nikel near disilicide))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/06/16 15:38

US-PAT-NO: 5882998

DOCUMENT-IDENTIFIER: US 5882998 A

TITLE: Low power programmable **fuse** structures and methods for making the same

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Abstract Text - ABTX (1):

Disclosed is a semiconductor **fuse** structure having a low power **programming** threshold and anti-reverse engineering characteristics. The **fuse** structure includes a substrate having a field oxide region. A polysilicon strip that has an increased dopant concentration region lies over the field oxide region. The **fuse** structure further includes a silicided metallization layer having first and second regions lying over the polysilicon strip. The first region has a first thickness, and the second region has a second thickness that is less than the first thickness and is positioned substantially over the increased dopant concentration region of the polysilicon strip. Preferably, the first region of the silicided metallization layer has a first side and a second side located on opposite sides of the second region, and the resulting **fuse** structure is substantially rectangular in shape. Therefore, the semiconductor **fuse** structure can be **programmed** by breaking the second region.

Application Filing Date - AD (1):

19980403

TITLE - TI (1):

Low power programmable **fuse** structures and methods for making the same

Brief Summary Text - BSTX (5):

There are a significant number of integrated circuit applications that require some sort of electrically programmable memory for storing

information.
The information stored varies widely in size ranging from a few bits used to
program simple identification data, to several megabits used to **program**
computer operating code. To accommodate the increased demand for electrically
programmable memory in modern integrated circuits, a number of well known
memory technologies that include, for example, programmable read only memories
(PROMs), erasable programmable read-only memories (EPROMs), electrically
erasable programmable read-only memories (EEPROMs), field programmable gate
arrays (FPGAs), and antifuse devices have been readily used. However,
fabricating these types of memory devices along with core logic integrated
circuitry adds a number of additional processing steps that unfortunately drive
up product costs. The additional product costs are often times difficult to
justify when only relatively small amounts of electrically programmable
elements are needed for a particular integrated circuit application.

Brief Summary Text - BSTX (6):
To reduce costs, semiconductor designers have been implementing "**fuse**"
structures that are made out of existing doped polysilicon layers that are
typically patterned to define transistor gates over a semiconductor structure.
Once formed, the **fuse** structure may be "**programmed**" by passing a sufficiently
high **current** that melts and vaporizes a portion of the polysilicon **fuse**. In
the **programmed** state, the **fuse** structure typically has a **resistance** that is
substantially greater than the non-**programmed** state, thereby producing an open
circuit. This is of course counter to antifuse devices that become short
circuits (i.e., substantially decreased **resistance) in a programmed** state.
Although traditional **fuse** structures work well, they typically consume a large
amount of power in **programming** that may make them unfit for a variety of low

power integrated circuit products.

Brief Summary Text - BSTX (7):
For example, the power dissipated in **programming a fuse** structure is given
by the expression V.sup.2 /R, where V is the **voltage** applied to the **fuse,** and R
is the **resistance**. As is well known, the applied **voltage** must be sufficiently
large in order to cause a **programming** event (e.g., produce an open circuit) in
the doped polysilicon **fuse** structure. Oftentimes, these **voltage** levels may be
larger than the power supplies used by many advanced integrated circuits.

Brief Summary Text - BSTX (8):
Besides consuming substantial amounts of power to cause the doped
polysilicon **fuse** structure to be **programmed,** special high **voltage** transistors
are typically designed routed and interconnected over the semiconductor chip
itself to direct the increased **programming voltages** to selected **fuses**.
Consequently, the special high **voltage** transistors occupy additional chip
surface area, thereby causing an increase in chip dimensions, and thereby
increasing product costs.

Brief Summary Text - BSTX (9):
Further, **fuse** technology has been gaining increased popularity in a variety
of consumer electronics, that store confidential information such as pin
numbers, bank account numbers, social security numbers and other confidential
information directly on a chip. Because this type of information is of such
confidential nature, it is critical that such integrated products having **fuse**
programmed data be difficult to reverse engineer. However, a number of **fuse**
structures having distinct advantages are patterned in distinguishing "bow-tie"
shapes to facilitate **programming** in the vicinity of a narrow neck area. For
more information on the advantages of bow-tie shaped **fuse** structures, reference
may be made to co-pending U.S. patent application Ser. No.

08/774,036, which is incorporated by reference herein. Although the narrow neck area facilitates **programming,** it also makes **fuse** detection rather straight forward for persons attempting to reverse engineer the **fuse** structures to illegally gain access to confidential information **programmed** therein.

Brief Summary Text - BSTX (10):
Accordingly, in view of the foregoing, there is a need for a method of fabricating **fuse** structures that utilize relatively small amounts of **programming** power and are difficult to identify during improper reverse engineering attempts.

Brief Summary Text - BSTX (12):
Broadly speaking, the present invention fills these needs by providing a **fuse** structure and method for making a **fuse** structure that has low **programming** power consumption characteristics and is difficult to distinguish from other semiconductor features patterned over a semiconductor die. It should be appreciated that the present invention can be implemented in numerous ways, including as a process, an apparatus, a system, a device, or a method. Several inventive embodiments of the present invention are described below.

Brief Summary Text - BSTX (13):
In one embodiment, a semiconductor **fuse** structure having a low power **programming** threshold is disclosed. The **fuse** structure includes a substrate having a field oxide region. A polysilicon strip that has an increased dopant concentration region that lies over the field oxide region. The **fuse** structure further includes a silicided metallization layer having first and second regions lying over the polysilicon strip. The first region has a first thickness, and the second region has a second thickness that is less than the first thickness and is positioned substantially over the increased dopant concentration region of the polysilicon strip. Preferably, the first

In the example of FIG. 6, a **current** "I" is shown flowing from metallization line 38b to 38a, and therefore, the electrons will flow from metallization line 38a to 38b. Because silicided layer 30 has a sheet **resistance** that is substantially lower than the underlying polysilicon strip 14, the bulk of the **current** will be carried by silicide layer 30. Because the **current** bulk is carried in silicide layer 30, the **current** generated joule heat will cause a net electromigration of tungsten silicide in the direction of electronic flow.

Detailed Description Text - DETX (19):

In a matter of a few microseconds, the migration of tungsten silicide will become so large that a break will occur in the silicide layer 30. In a preferred embodiment, the **programming** pulse width is between about 100 microseconds and about 500 milliseconds, and more preferably between about 1 millisecond and about 100 milliseconds, and most preferably about 50 milliseconds. Because the applied **programming** pulse is substantially smaller than the **programming** pulse widths of typical **fuse** structures, the power consumed in **programming fuse** structure in accordance with one embodiment of the present invention is substantially reduced.

Detailed Description Text - DETX (20):

FIG. 7 shows the **fuse** structure 40 after **programming** in accordance with one embodiment of the present invention. By way of example, the **programmed fuse** structure 40 will have a gap 32' in the thinner region of the silicide layer 30. As mentioned earlier, the **programming current** flow through the thinner region caused the increase in joule heat that vaporized the silicide layer. As pictorially illustrated, once **programmed, the current** "I" will not longer flow through the low sheet resistive silicide layer 30 due to the gap 32', and will suddenly be forced to flow through a more highly resistive polysilicon strip

14. Because the **resistance** is substantially higher in the underlying polysilicon strip 14, the **fuse** structure 40 will respond as an open circuit.
It therefore follows that substantially less power is consumed in arriving at a **programmed fuse** structure state.

Detailed Description Text - DETX (21):
FIG. 8A is a top view of the bi-layer **fuse** structure 40 formed over field oxide 12 in accordance with one embodiment of the present invention. Preferably **fuse** structure 40 is substantially rectangular in shape having a longer side that is X*Lmin, where Lmin is between about 700 angstroms and about 20,000 angstroms, and more preferably about 1,500 angstroms and about 5,000 angstroms, and most preferably about 2,500 angstroms. The shorter side of **fuse** structure 40 is about Lmin, and so is the distance between contacts 36 and the thin silicide region 32. Therefore, the thin silicided region 32 may be square shaped in some embodiments, and in other embodiments, thin silicided region 32 may be rectangular. In any event, the longer side of the **fuse** structure 40 is about 5*Lmin, where X=5. It should be appreciated that the preferred rectangular shape of **fuse** structure 40 may have slightly rounded ends and may have a center region that is less than Lmin (i.e., <Lmin) as shown in FIG. 8B.

Detailed Description Text - DETX (22):
FIG. 9 illustrates a bi-layer **fuse** structure including a polysilicon strip 14 and an overlying silicide layer 30 in accordance with an alternative embodiment of the present invention. In this embodiment, the doped polysilicon strip 14 is not masked and doped with an increased concentration before forming the silicide layer 30. However, as shown in FIG. 10, a photoresist mask 50 is patterned over the silicide layer 30 to define a window 16" that preferably exposes a region that lies approximately at the center of the bi-layer **fuse** structure. Next, a time controlled etch is performed to etch about

half the
thickness of the silicide layer 30 lying within the window 16" in the
photoresist mask 50.

Detailed Description Text - DETX (25):
FIG. 11 illustrates the **fuse** structure 40' after the photoresist layer 50 is
removed after an etching step in accordance with the alternative embodiment of
the present invention. As in the embodiment of FIG. 5A; a thin silicided
region 32 results with thicker silicided regions on either side of the thin
region. Having this thinner region therefore enable **programming of the fuse**
structure 40' with substantially less power than conventional **fuse**
structures.

Detailed Description Text - DETX (26):
FIG. 12 illustrates the final **fuse** structure 40' having contacts 36
connected to each respective side of the silicide layer 30 in accordance with
the alternative embodiment of the present invention. Therefore, as described
above with reference to FIG. 6, the bulk of the **programming current** "I" will
naturally flow through the less resistive silicide layer 30 while
simultaneously generating increased joule heat near the thin silicide region 32
that rapidly causes a **programming** break in the silicide layer 30. Once the gap
32' (i.e., a vaporized electromigration break) occurs in the thin silicide
region 32, the **current** will be forced to flow through the underlying
polysilicon strip 14 as illustrated in FIG. 13.

Detailed Description Text - DETX (27):
Because the sheet **resistance** of the polysilicon strip 14 can be as high as
about 100 .OMEGA./.quadrature., the **fuse** will respond substantially like a open
circuit in its **programmed** state. It is again noted that the thin silicide
region 32 in the **fuse** structure 40' advantageously assists in consuming
substantially less power as well as achieving much more rapid **programming**
times. In addition, because **fuse** structures, are more frequently being used to

store highly confidential data, it is very important that the reverse engineering of **programmed fuse** structures be made as difficult as possible. As
described above, the layout geometries of the **fuse** structures of the present
invention are substantially similar to a number of other very common semiconductor device features, which may include for example, transistor gates,
device interconnect jumpers, or even metallization routing lines. Therefore,
identifying which geometries are or are not **fuse** structures is advantageously
made very laborious and costly.

Claims Text - CLTX (1):
1. A method of making a low power programmable **fuse** structure, comprising:

Claims Text - CLTX (7):
2. A method of making a low power programmable **fuse** structure as recited in
claim 1, wherein the forming the doped polysilicon strip further comprises:

Claims Text - CLTX (10):
3. A method of making a low power programmable **fuse** structure as recited in
claim 2, wherein the thinner layer of the silicide metal that is formed over
the increased dopant concentration region is about half the thickness of the
thicker layer of the silicide metal that is formed over other regions of the
doped polysilicon strip, and the other regions being integrally adjacent to the
thinner layer.

Claims Text - CLTX (11):
4. A method of making a low power programmable **fuse** structure as recited in
claim 2, wherein the short side of the substantially rectangular shape is
between about 1,500 angstroms and about 5,000 angstroms.

Claims Text - CLTX (12):
5. A method of making a low power programmable **fuse** structure as recited in
claim 4, wherein the increased dopant concentration region has a concentration
of between about 3.times.10.sup.20 atoms cm.sup.-3 and about